

NBSG11

2.5V/3.3V SiGe 1:2 Differential Clock Driver with RSECL* Outputs

*Reduced Swing ECL

The SG11 is a Silicon Germanium 1-to-2 differential fanout buffer, optimized for low skew and ultra-low JITTER.

Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV.

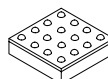
- Maximum Input Clock Frequency > 12 GHz Typical
- 30 ps Typical Rise and Fall Times
- 125 ps Typical Propagation Delay
- RSPECL Output with Operating Range: $V_{CC} = 2.375\text{ V}$ to 3.465 V with $V_{EE} = 0\text{ V}$
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: $V_{CC} = 0\text{ V}$ with $V_{EE} = -2.375\text{ V}$ to -3.465 V
- RSECL Output Level (400 mV Peak-to-Peak Output), Differential Output Only
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LEVEL Devices



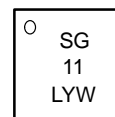
ON Semiconductor™

<http://onsemi.com>

MARKING DIAGRAM*



FCBGA-16
BA SUFFIX
CASE 489



L = Wafer Lot
Y = Year
W = Work Week

*For further details, refer to Application Note
AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NBSG11BA	4x4 mm FCBGA-16	100 Units/Tray
NBSG11BAR2	4x4 mm FCBGA-16	500/Tape & Reel

Board	Description
SG11EVB	NBSG11BA Evaluation Board

NBSG11

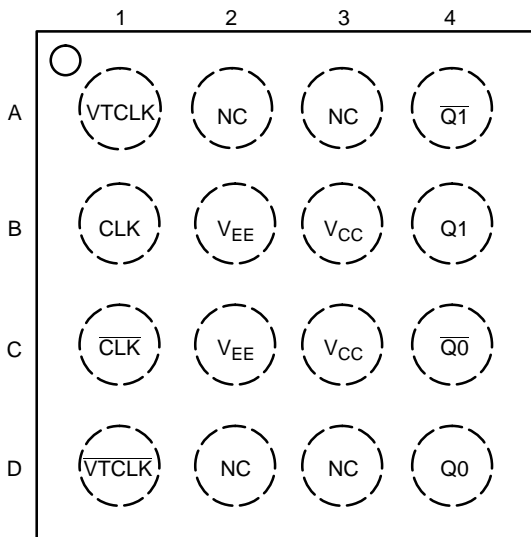


Figure 1. Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
CLK*, $\overline{\text{CLK}}$ **	ECL, TTL, CMOS, CML, LVDS compatible (CLK) inputs
Q0, $\overline{\text{Q0}}$ Q1, $\overline{\text{Q1}}$	RSECL Data Outputs
VTCLK, $\overline{\text{VTCLK}}$	50 Ω Internal Input Termination Resistor
V _{CC}	Positive Supply
V _{EE}	Negative Supply
NC	No Connect

* Pin will default low when left open.

** Pin will default to a slightly higher potential than CLK when both are left open.

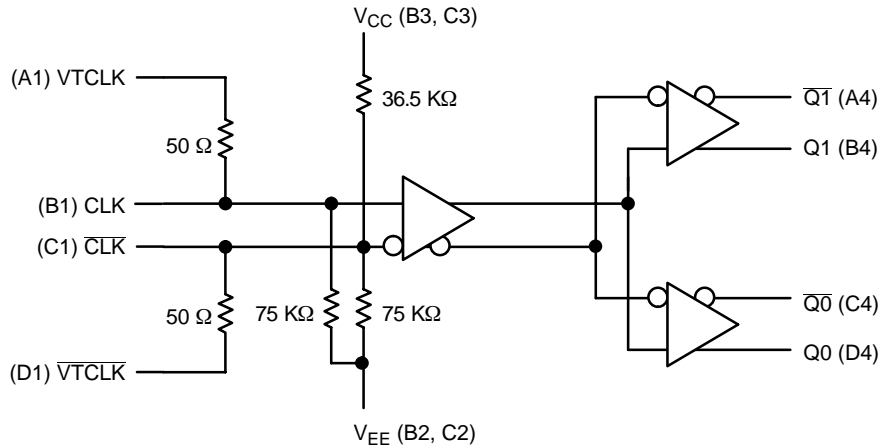


Figure 2. Logic Diagram

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK and $\overline{\text{VTCLK}}$ to V _{CC}
LVDS	Connect VTCLK and $\overline{\text{VTCLK}}$ together
AC-COUPLED	Bias VTCLK and $\overline{\text{VTCLK}}$ Inputs within (VIHCMR) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques

NBSG11

ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor (CLK, $\overline{\text{CLK}}$)	75 k Ω
Internal Input Pullup Resistor ($\overline{\text{CLK}}$)	36.5 k Ω
ESD Protection	Human Body Model Machine Model
	> 2 kV > 100 V
Moisture Sensitivity (Note 1)	Level 3
Flammability Rating	UL 94 V-0 @ 0.125"
Oxygen Index	28 to 34
Transistor Count	125
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	Positive Power Supply	V _{EE} = 0 V		3.6	V
V _{EE}	Negative Power Supply	V _{CC} = 0 V		-3.6	V
V _I	Positive Input Negative Input	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	3.6 -3.6	V V
I _{out}	Output Current	Continuous Surge		25 50	mA mA
T _A	Operating Temperature Range			-40 to +70	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 LFPM 500 LFPM	16 FCBGA 16 FCBGA	108 86	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	1S2P (Note 3)	16 FCBGA	5	°C/W
T _{sol}	Wave Solder	< 15 Seconds		225	°C

2. Maximum Ratings are those values beyond which device damage may occur.

3. JEDEC standard multilayer board – 1S2P (1 signal, 2 power).

NBSG11

DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT $V_{CC} = 2.5\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 4)

Symbol	Characteristic	-40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 5)	1450	1530	1575	1525	1565	1600	1550	1590	1625	mV
V_{OUTpp}	Output p-p Voltage	350	410	525	350	410	525	350	410	525	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 7)	$V_{CC} - 1435\text{ mV}$	$V_{CC} - 1000\text{ mV}^*$	V_{CC}	$V_{CC} - 1435\text{ mV}$	$V_{CC} - 1000\text{ mV}^*$	V_{CC}	$V_{CC} - 1435\text{ mV}$	$V_{CC} - 1000\text{ mV}^*$	V_{CC}	V
V_{IL}	Input LOW Voltage (Single-Ended) (Note 8)	$V_{IH} - 2.5\text{ V}$	$V_{CC} - 1400\text{ mV}^*$	$V_{IH} - 150\text{ mV}$	$V_{IH} - 2.5\text{ V}$	$V_{CC} - 1400\text{ mV}^*$	$V_{IH} - 150\text{ mV}$	$V_{IH} - 2.5\text{ V}$	$V_{CC} - 1400\text{ mV}^*$	$V_{IH} - 150\text{ mV}$	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)	1.2		2.5	1.2		2.5	1.2		2.5	V
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH} , V_{IHMAX})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL} , V_{ILMIN})		25	100		25	100		25	100	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

4. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.125 V to -0.965 V.
 5. All loading with 50 Ω to $V_{CC} - 2.0$ volts. V_{OH}/V_{OL} measured at V_{IH}/V_{IL} .
 6. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
 7. V_{IH} cannot exceed V_{CC} .
 8. V_{IL} always $\geq V_{EE}$.
- *Typicals used for testing purposes.

DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT $V_{CC} = 3.3\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 9)

Symbol	Characteristic	-40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 10)	2250	2330	2375	2325	2365	2400	2350	2390	2425	mV
V_{OUTpp}	Output p-p Voltage	350	410	525	350	410	525	350	410	525	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 12)	$V_{CC} - 1435\text{ mV}$	$V_{CC} - 1000\text{ mV}^*$	V_{CC}	$V_{CC} - 1435\text{ mV}$	$V_{CC} - 1000\text{ mV}^*$	V_{CC}	$V_{CC} - 1435\text{ mV}$	$V_{CC} - 1000\text{ mV}^*$	V_{CC}	V
V_{IL}	Input LOW Voltage (Single-Ended) (Note 13)	$V_{IH} - 2.5\text{ V}$	$V_{CC} - 1400\text{ mV}^*$	$V_{IH} - 150\text{ mV}$	$V_{IH} - 2.5\text{ V}$	$V_{CC} - 1400\text{ mV}^*$	$V_{IH} - 150\text{ mV}$	$V_{IH} - 2.5\text{ V}$	$V_{CC} - 1400\text{ mV}^*$	$V_{IH} - 150\text{ mV}$	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 11)	1.2		3.3	1.2		3.3	1.2		3.3	V
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH} , V_{IHMAX})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL} , V_{ILMIN})		25	100		25	100		25	100	μA

NOTE: SiGe Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

9. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925 V to -0.165 V.
 10. All loading with 50 Ω to $V_{CC} - 2.0$ volts. V_{OH}/V_{OL} measured at V_{IH}/V_{IL} .
 11. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
 12. V_{IH} cannot exceed V_{CC} .
 13. V_{IL} always $\geq V_{EE}$.
- *Typicals used for testing purposes.

NBSG11

DC CHARACTERISTICS, NECL OR RSNECL INPUT WITH NECL OUTPUT $V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V}$ to -2.375 V (Note 14)

Symbol	Characteristic	-40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 15)	-1050	-970	-925	-975	-935	-900	-950	-910	-875	mV
V_{OUTpp}	Output p-p Voltage	350	410	525	350	410	525	350	410	525	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 17)	$V_{CC}-1435\text{ mV}$	$V_{CC}-1000\text{ mV}^*$	V_{CC}	$V_{CC}-1435\text{ mV}$	$V_{CC}-1000\text{ mV}^*$	V_{CC}	$V_{CC}-1435\text{ mV}$	$V_{CC}-1000\text{ mV}^*$	V_{CC}	V
V_{IL}	Input LOW Voltage (Single-Ended) (Note 18)	$V_{IH}-2.5\text{ V}$	$V_{CC}-1400\text{ mV}^*$	$V_{IH}-150\text{ mV}$	$V_{IH}-2.5\text{ V}$	$V_{CC}-1400\text{ mV}^*$	$V_{IH}-150\text{ mV}$	$V_{IH}-2.5\text{ V}$	$V_{CC}-1400\text{ mV}^*$	$V_{IH}-150\text{ mV}$	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 16)	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	V
I_{IH}	Input HIGH Current (@ V_{IH} , V_{IHMAX})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL} , V_{ILMIN})		25	100		25	100		25	100	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

14. Input and output parameters vary 1:1 with V_{CC} .

15. All loading with $50\ \Omega$ to $V_{CC}-2.0$ volts. V_{OH}/V_{OL} measured at V_{IH}/V_{IL} .

16. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

17. V_{IH} cannot exceed V_{CC} .

18. V_{IL} always $\geq V_{EE}$.

*Typicals used for testing purposes.

AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V}$ to -2.375 V or $V_{CC} = 2.375\text{ V}$ to 3.465 V ; $V_{EE} = 0\text{ V}$

Symbol	Characteristic	-40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 3. $F_{max}/JITTER$) (Note 19)	10.709	> 12		10.709	> 12		10.709	> 12		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential	90	125	160	90	125	160	90	125	160	ps
t_{SKEW}	Duty Cycle Skew (Note 20) Within-Device Skew (Note 21) Device-to-Device Skew (Note 22)		3 6 25	15 15 50		3 6 25	15 15 50		3 6 25	15 15 50	ps
t_{JITTER}	Cycle-to-Cycle Jitter (RMS) (See Figure 3. $F_{max}/JITTER$) (Note 19)		0.5	< 1		0.5	< 1		0.5	< 1	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential) (Note 23)	75		2600	75		2600	75		2600	mV
t_r , t_f	Output Rise/Fall Times (20% - 80%) Q, \bar{Q}	20	30	55	20	30	55	20	30	55	ps

19. Measured using a 500 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC}-2.0\text{ V}$. For minimum f_{max} value of 10.709 GHz, output amplitude is approximately 200 mV (as shown in Figure 3, where output P-P spec is shown as a minimum/guarantee of around 150 mV).

20. See Figure 4. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% Differential Clock Input Waveform.

21. Within-Device skew is defined as identical transitions on similar paths through a device.

22. Device-to-device skew for identical transitions at identical V_{CC} levels.

23. V_{INpp} (MAX) cannot exceed $V_{CC} - V_{EE}$.

NBSG11

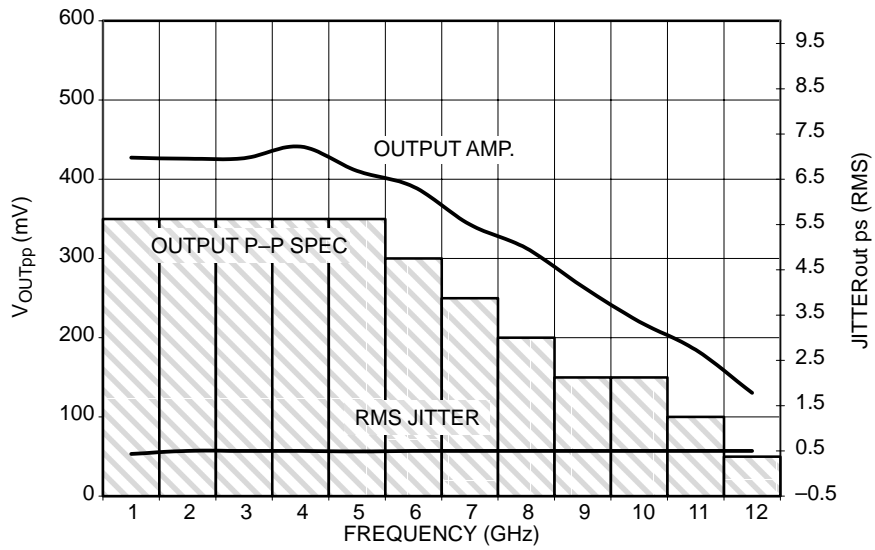


Figure 3. F_{max}/Jitter

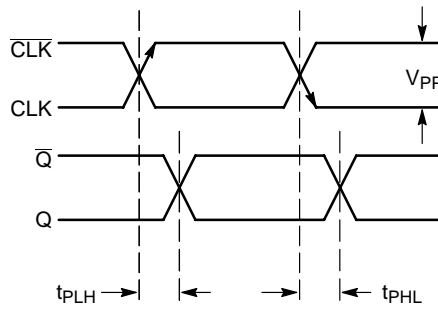


Figure 4. AC Reference Measurement

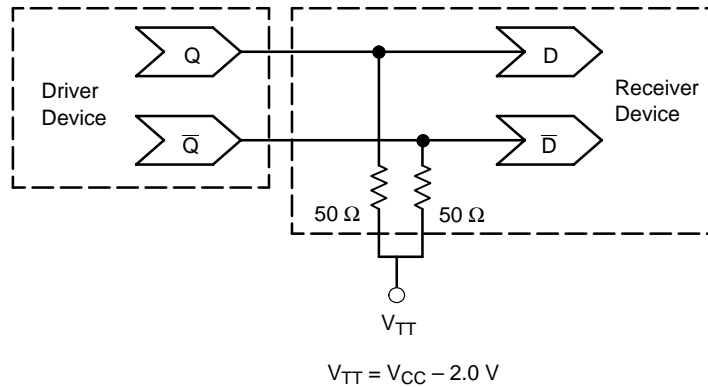
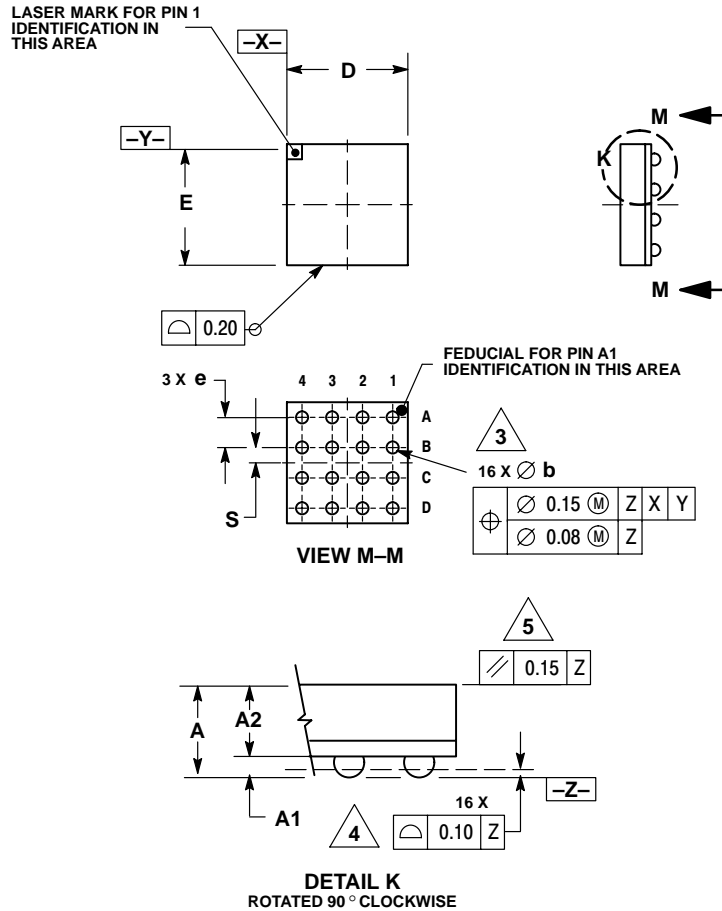


Figure 5. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 – Termination of ECL Logic Devices)

NBSG11

PACKAGE DIMENSIONS


**FCBGA-16
BA SUFFIX**
PLASTIC 4X4 (mm) BGA FLIP CHIP PACKAGE
CASE 489-01
ISSUE O



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

DIM	MILLIMETERS	
	MIN	MAX
A	1.40	MAX
A1	0.25	0.35
A2	1.20	REF
b	0.30	0.50
D	4.00	BSC
E	4.00	BSC
e	1.00	BSC
S	0.50	BSC

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.